



FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE  
STATEMENT BY APPLICANT  
(37 CFR 1.98(b))Attorney Docket No.:  
L&L-I0232Applic. No.  
10/047,013

Applicant

Wolfgang Rösner et al.

Filing Date  
January 16, 2002Group Art Unit  
2811

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
PF	A	5,714,766	02/03/98	Chen et al.			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

## FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
PF	J	196 32 835 C1	04/02/98	Germany			X
PF	K	0 843 361 A1	05/20/98	Europe			X
	L						
	M						
	N						

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

PF	O	H.I. Liu et al.: "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires", Appl. Phys. Lett., Vol. 64, No. 11, March 14, 1994, pp. 1383-1385
Re	P	Harald Gossner et al.: "Vertical Si-Metal-Oxide-Semiconductor Field Effect Transistors with Channel Lengths of 50 nm by Molecular Beam Epitaxy", Jpn. J. Appl. Phys., Vol. 33, 1994, pp. 2423-2428

EXAMINER

*SMH* *Rosen*

DATE CONSIDERED

*04/21/02*

EXAMINER: Initial citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



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LB	O	Lothar Risch et al.: "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498
fb	P	Hiroshi Fukuda et al.: "Fabrication of silicon nanopillars containing polycrystalline silicon/insulator multilayer structures", Appl. Phys. Lett., Vol. 70, No. 3, January 20, 1997, pp. 333-335

EXAMINER

RPL L RAN RAN

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04/01/07

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STATEMENT BY APPLICANT  
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L&L-10232Applic. No.  
10/047,013

Applicant

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## U.S. PATENT DOCUMENTS

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

P6	O	Hiroshi Mizuta et al.: "High-speed single-electron memory: cell design and architecture", XP-002151823, IEEE 1998, pp. 67-72
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*SLH*

PATT. EXAM.

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04/01/03

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